

P-Channel 20-V (D-S) MOSFET

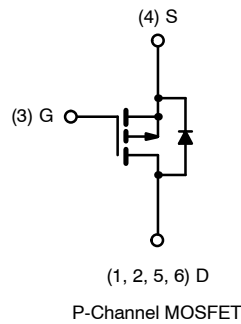
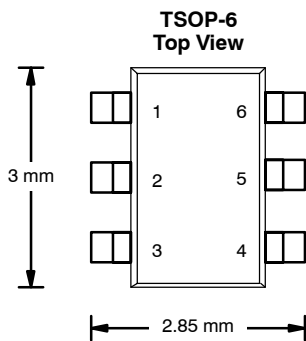
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-20	0.030 @ $V_{GS} = -10$ V	-6.7
	0.051 @ $V_{GS} = -4.5$ V	-5.1

FEATURES

- TrenchFET® Power MOSFET

APPLICATIONS

- Load Switch
 - Notebook PC
 - Game Machine
 - Desktop



Ordering Information: Si3469DV-T1—E3 (Lead Free)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	5 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	-20		V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	-6.7	-5.0	A
		$T_A = 70^\circ\text{C}$	-5.3	-4.0	
Pulsed Drain Current	I_{DM}	-25			
Continuous Source Current (Diode Conduction) ^a	I_S	-1.7	-0.95		
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	2.0	1.14	W
		$T_A = 70^\circ\text{C}$	1.3	0.73	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 5$ sec	R_{thJA}	45	62.5	$^\circ\text{C/W}$
	Steady State		90	110	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	25	30	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

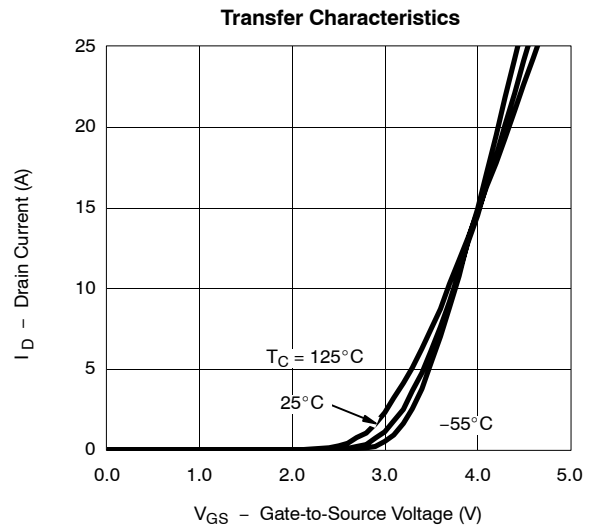
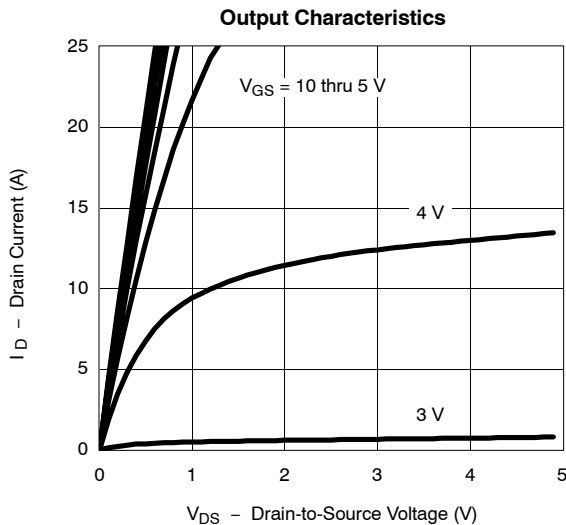


SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-1.0		-3	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -20 V, V _{GS} = 0 V, T _J = 85 °C			-5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = -10 V	-25			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -10 V, I _D = -6.7 A		0.024	0.030	Ω
		V _{GS} = -4.5 V, I _D = -2 A		0.041	0.051	
Forward Transconductance ^a	g _{fs}	V _{DS} = -15 V, I _D = -6.7 A		15		S
Diode Forward Voltage ^a	V _{SD}	I _S = -1.7 A, V _{GS} = 0 V		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = -10 V, V _{GS} = -10 V, I _D = -6.7 A		20	30	nC
Gate-Source Charge	Q _{gs}			3.8		
Gate-Drain Charge	Q _{gd}			4.8		
Gate Resistance	R _g	f = 1 MHz		9		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = -10 V, R _L = 10 Ω I _D ≈ -1 A, V _{GEN} = -10 V, R _G = 6 Ω		10	15	ns
Rise Time	t _r			12	20	
Turn-Off Delay Time	t _{d(off)}			50	75	
Fall Time	t _f			35	55	
Source-Drain Reverse Recovery Time	t _{rr}		I _F = -1.7 A, di/dt = 100 A/μs		25	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

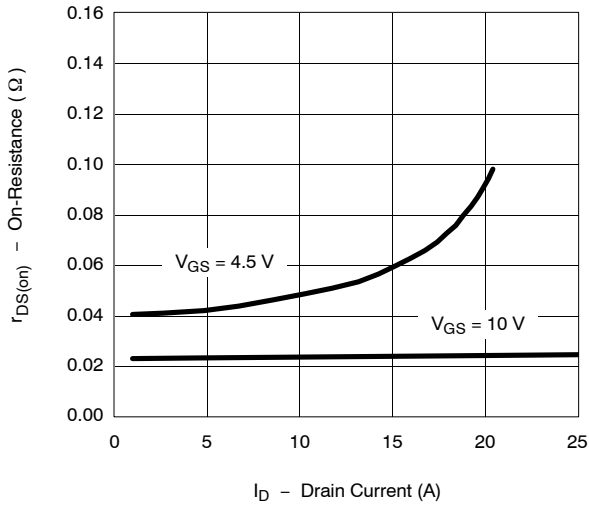
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



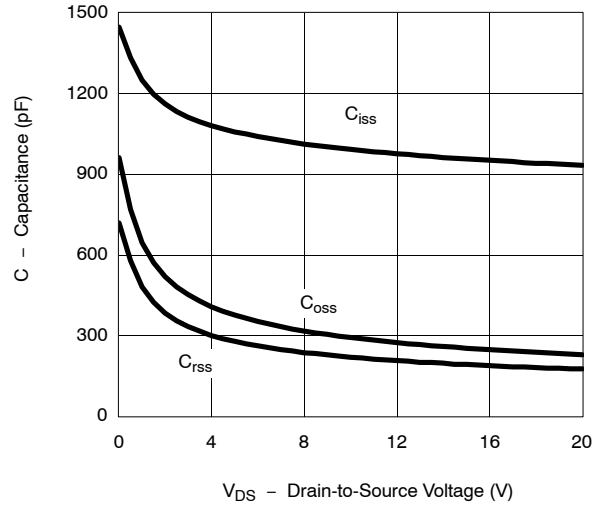


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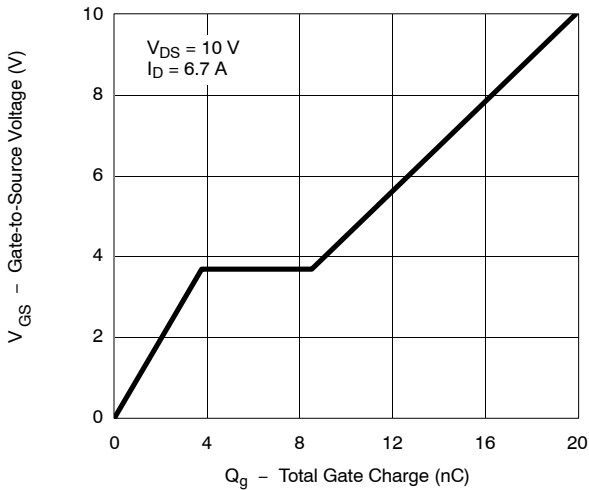
On-Resistance vs. Drain Current



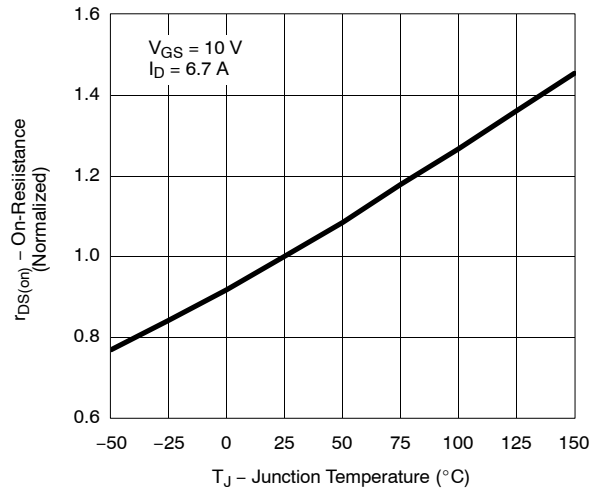
Capacitance



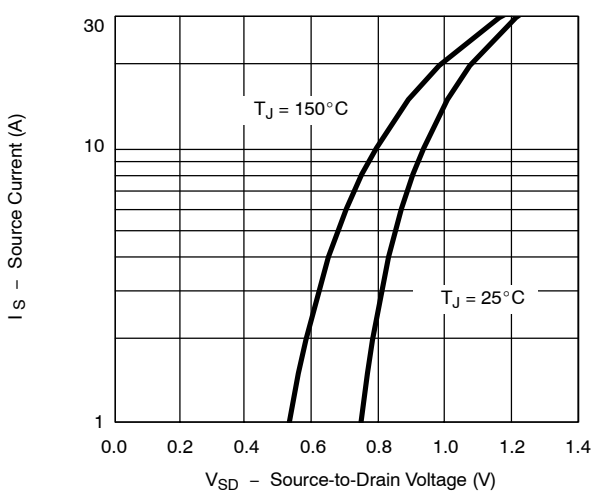
Gate Charge



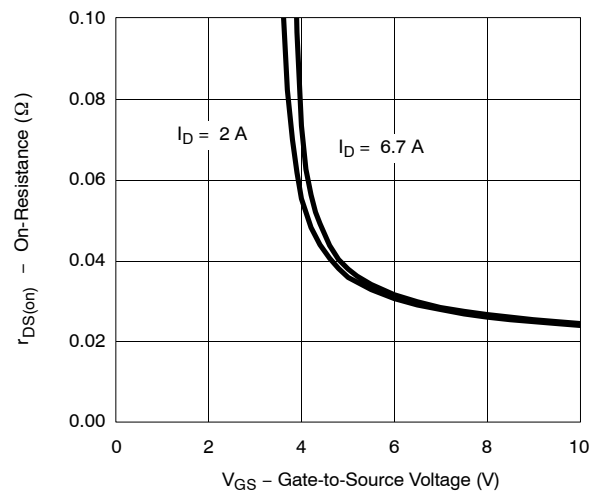
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

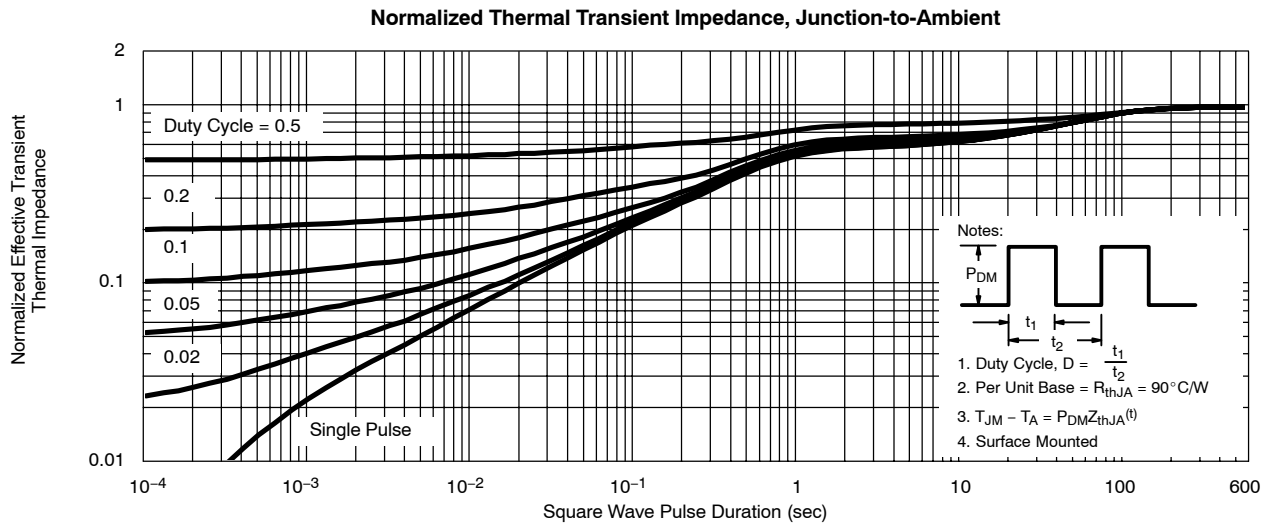
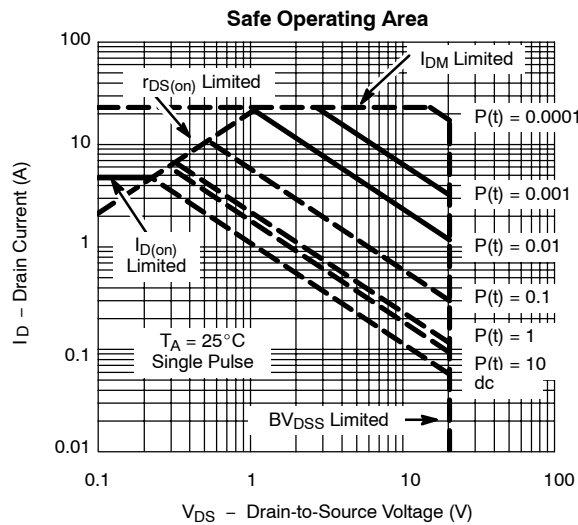
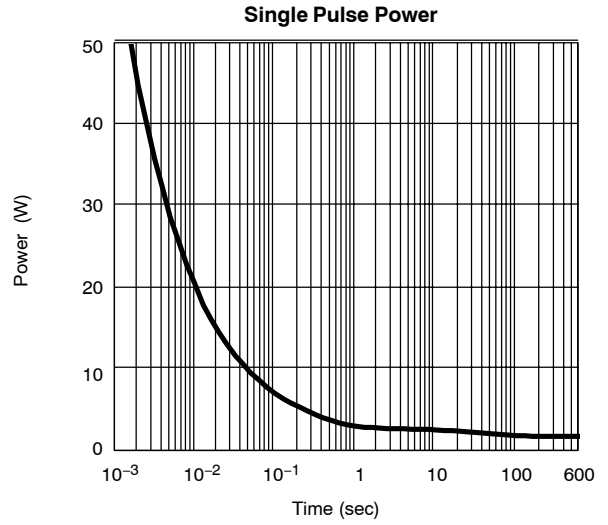
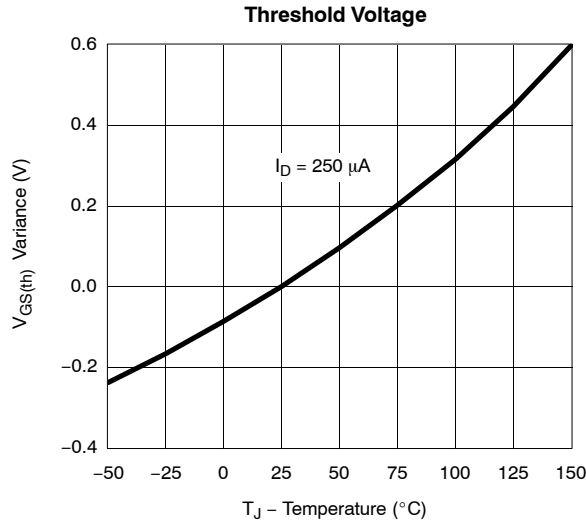


On-Resistance vs. Gate-to-Source Voltage



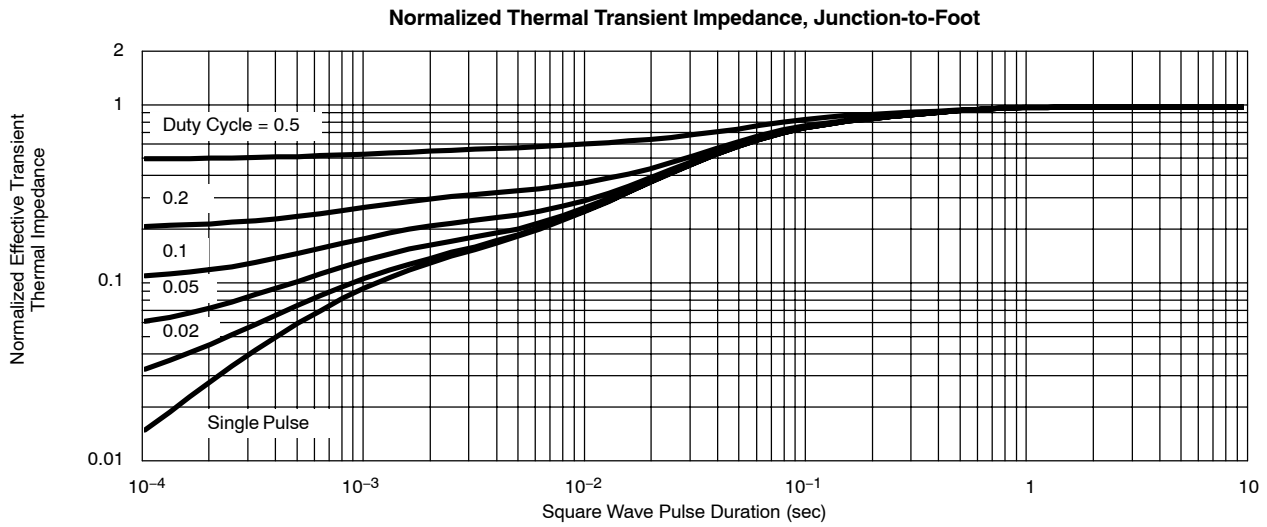


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)





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